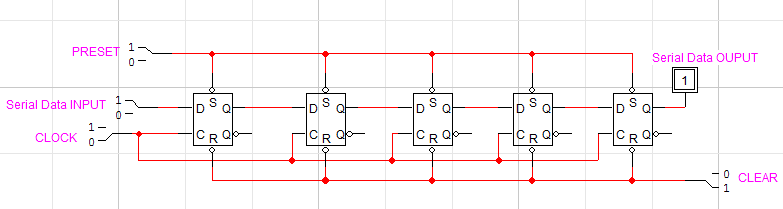
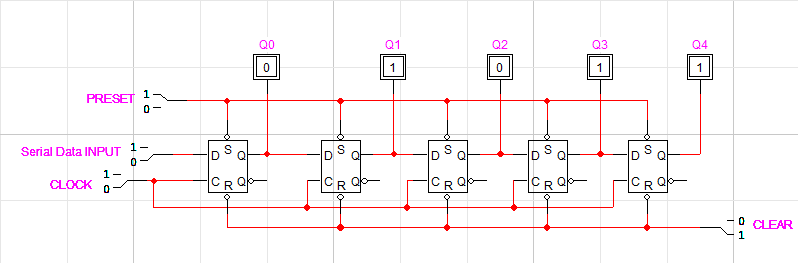
**DLD Lab 13**

Q1) Implement the following 5-BIT registers using D-Flip-flop.

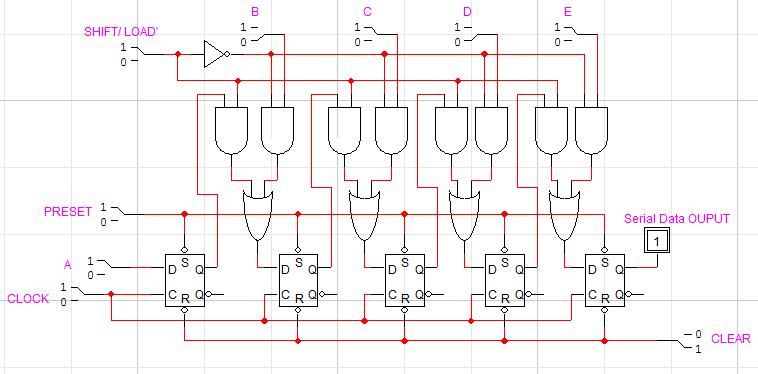
1. Serial In Serial Out (SISO) Serial In



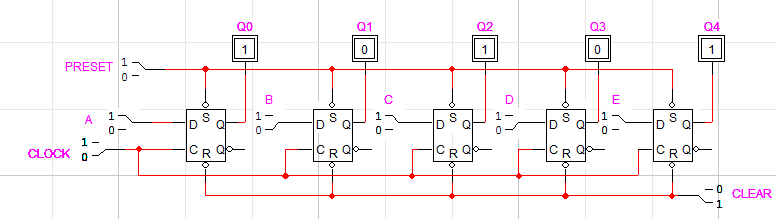
1. Parallel Out (SIPO) Parallel In Serial



1. Out (PISO) Parallel In Parallel Out

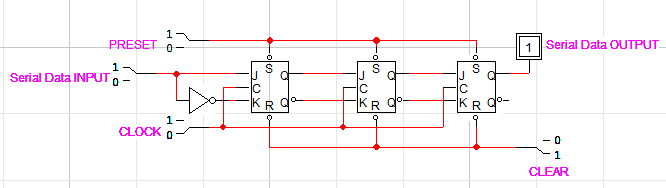


1. (PIPO)

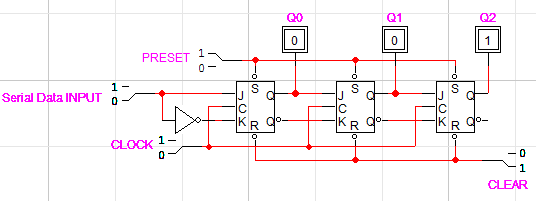


Q2) Implement the following 3-BIT registers using JK-Flip-flop.

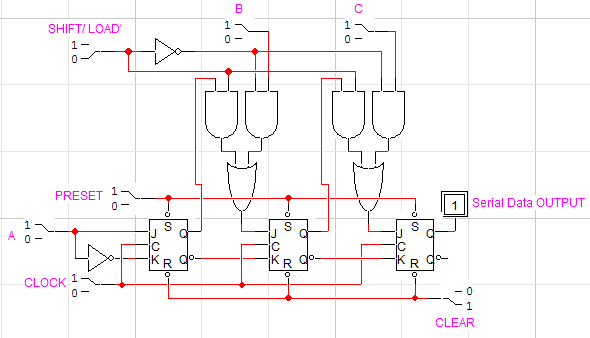
1. Serial In Serial Out (SISO)



1. Serial In Parallel Out (SIPO)



1. Parallel In Serial Out (PISO)



1. Parallel In Parallel Out (PIPO)

